

ROHM AND HAAS ELECTRONIC MATERIALS

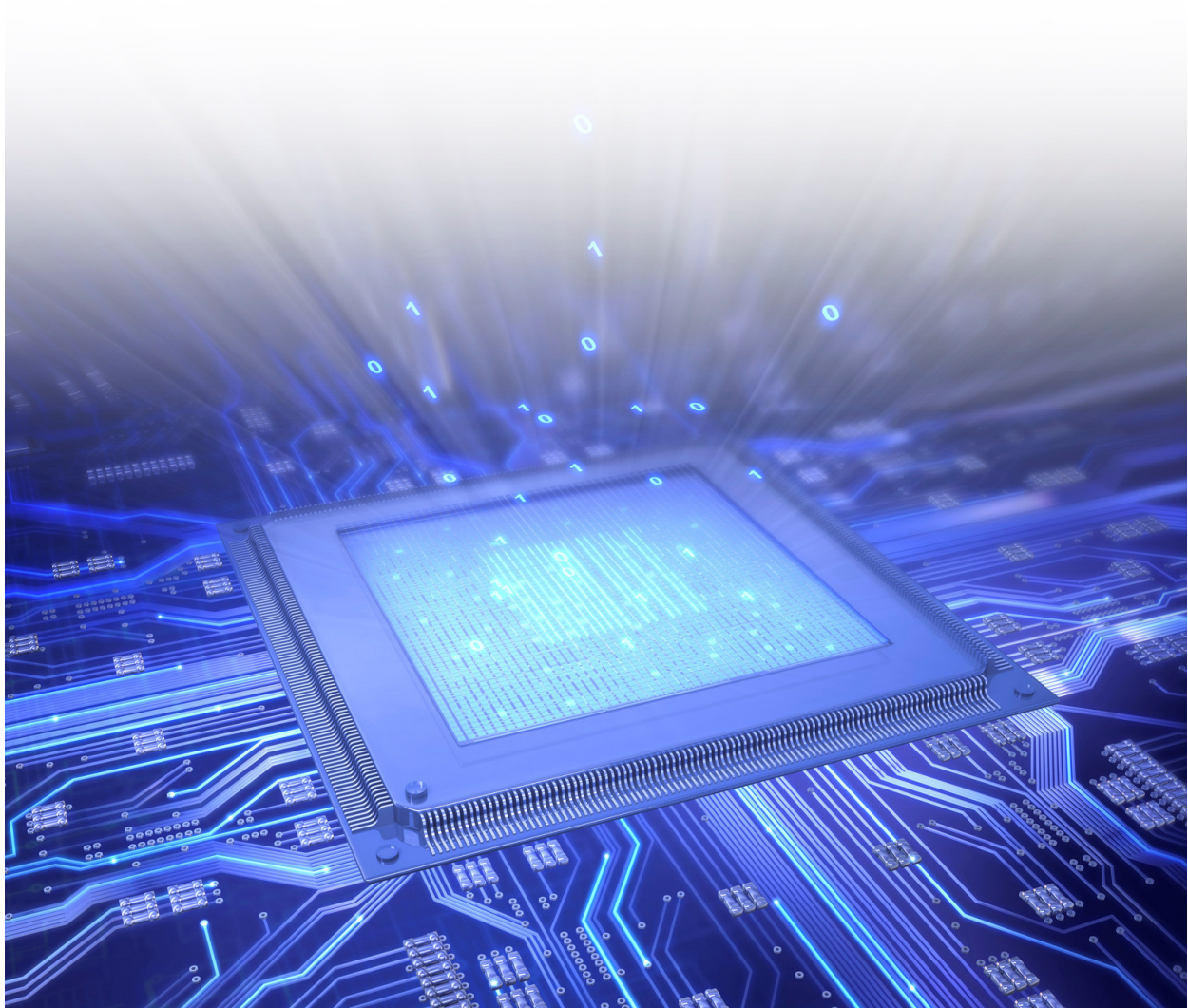
CIRCUIT BOARD TECHNOLOGIES

Technical Communications

Solder Joint Reliability

July 2008

This article is currently published at PCB007 website



Solder Joint Reliability

All over the world, every time that a cell phone or PDA drops onto a hard sidewalk, its owner, fearing the worst, breathes a sigh of relief when it survives the fall.

The complex interactions that make up solder joint reliability demand attention be paid to a multitude of different factors and requires that selections of materials are based on appropriate test methods and qualification.

The market requirements to increase system complexity, while simultaneously reducing product design cycle time, continue to drive use of denser integration of separate semiconductor die in system in package (SIP) formats. The internal connections

within an SIP may be made by either flip chip soldering or wire bonding or a combination of the two approaches. Continued evolution of complex packages force PWB substrates to meet ever higher interconnection density targets.

For portable products, iNEMI Board Assembly group (1) projects that maximum component interconnection density will pass 700 per square cm by 2011, while minimum interconnection pitch will move below 0.3 mm. As pitch decreases, the physical area, volume and strength of each individual solder joint becomes smaller and the margin for error becomes lower.

Factors Influencing Solder Joint Reliability

Overall solder joint reliability is determined by the combination of service environment and system design.

The service environment will determine the temperature extremes which the product must endure, the frequency of power on / off cycling, and the possibility of specific mechanical shocks (for example, drop) or vibrational stresses.

From the system design side, a series of factors that include component and substrate physical properties, solder joint geometry, bulk solder alloy mechanical properties, the nature of the intermetallic compounds formed and their structure at the solder joint / pads interfaces are important. Cost limitations add additional constraints, forcing hard choices to be made.

The key characteristics for components and substrates are their relative coefficients of thermal expansion and their strength and resistance to flexure. As the system status changes, the temperatures of the component and substrate also change (but not always at the same rate). In an active condition, semiconductor die temperatures will be higher than that of the adjacent substrate.

The forces generated by expansion coefficient mismatch will be distributed by mechanisms such as substrate bending, which may put larger stresses on joints at the center of packages (typical for thinner organic substrates carrying stiff CSP devices) or by distortion of solder joints. For larger packages on more rigid substrates, the stress generated by mismatch will be highest within those solder joints furthest from the center of the package.

Solder joint geometry factors include pad size and shape and the placement of the pad with respect to solder mask. A preference for etch defined pads rather than solder mask defined pads has been expressed in some literature (2), since etch-defined pads allow a stronger solder fillet to extend around the corner of the pad and also enclose the pad side walls.

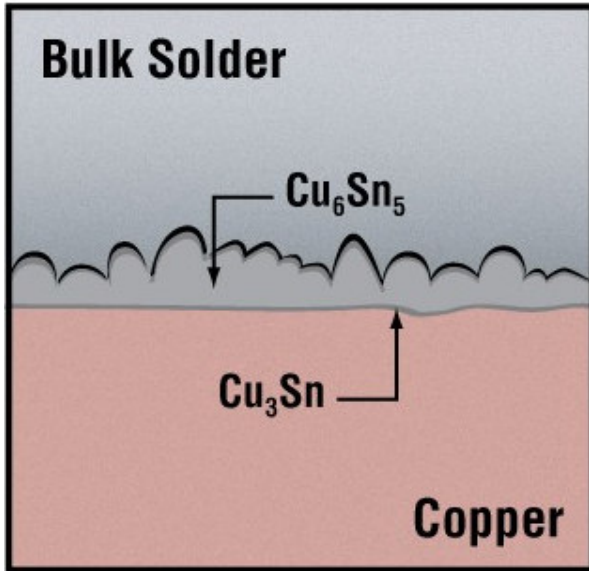
For solder alloys, eutectic tin-lead, with its long established history, has been replaced with the complexity of a multitude of new and unfamiliar lead-free alloys.

Modeling of solder joint reliability failure by solder fatigue or creep mechanisms is well documented for tin-lead alloy systems. The shift to lead-free has triggered a massive body of work to understand the ways in which the differences in physical properties and solder joint grain structures of these alloys lead to changes in failure mechanisms. From this basic information, appropriate models that connect measurements of material properties to anticipated reliability levels can be constructed. However failures that might occur due to deficiencies in surface wetting or interfacial intermetallic structure cannot be modeled using these approaches.

Formation of a strong and reliable solder joint is based on the ability of molten solder to rapidly and uniformly wet the surface finish and interact with it to form a consistent layer of intermetallic at the interface.

As shown schematically in Figure 1, in the case of solder joints formed on copper substrates, a layer of Cu_6Sn_5 is formed at the interface with bulk solder, while a thin layer of Cu_3Sn is present at the copper to intermetallic interface.

Figure 1: Schematic of Intermetallic Structure at Copper – Solder Interface



The thickness, composition and structure of intermetallic compounds formed at the solder joint / pad interfaces during assembly are controlled by three factors: the nature of the surface

finishes on the component and PWB substrate (including their cleanliness and condition), the solder alloy chosen, and by the assembly process conditions, including the flux used, reflow conditions and number of reflow cycles.

Individual joints within a single board may be formed under quite different thermal profiles due to differences in location within component (center versus edge of area array packages) or within the panel (in an open area versus adjacent to a high thermal mass component).

In addition, the initial intermetallic structure and thickness may also change significantly during service life, as diffusional processes continue slowly at both ambient and operating temperatures.

Intermetallic compounds such as the Cu_6Sn_5 / Cu_3Sn combination formed on most surface finishes, or the Ni_3Sn_4 , formed when soldering to nickel based finishes, are much harder and more brittle than copper or solder alloys. While some general rules can be drawn about interfacial structure, for example that the intermetallic should be adherent to the substrate and be substantially free of voids, correlation of IMC structure and thickness to reliability is a highly empirical exercise.

Test Methods

To avoid the difficulties of predicting solder joint reliability based on indirect metrics, in an ideal world, each individual product would be tested at the final assembled level to establish its capability. In the real world, design cycles do not allow this luxury,

and extrapolations from a variety of non-product specific tests have to be made.

Table 1 illustrates different levels at which information to predict solder joint reliability can be obtained.

Table 1: Solder Joint Reliability Prediction and Assessment Methods

Testing Approach	Typical Measurements	Test Conditions
Materials Level	Thickness / composition of surface finish Contamination levels	As-processed After multiple reflow cycles After accelerated aging
Processability Level	Solder spread Wetting time / force Solder dip coverage	As-processed After multiple reflow cycles After accelerated aging
Solder Reflow Level (without components)	Analysis of typical joint / IMC structure Shear / pull force Failure interface evaluation	As-processed After multiple reflow cycles After accelerated aging
Test Panel Level	Interconnect continuity Analysis of typical joint / IMC structure Failure interface evaluation	As-assembled After accelerated thermal or power cycling appropriate to application
Product Level	In-circuit test after assembly Analysis of failed joint / IMC structure	As-assembled After accelerated thermal / power cycling appropriate to application After field service

With so many established and novel options for surface finishes and so many approaches to providing reliability related information, it is a major task to master the different capabilities and limitations of individual finishes.

Component manufacturers, OEMs and academic laboratories are most likely to provide information at the test panel level. This type of data provides clear information on the capability of specific materials for an individual application.

Publications from these studies are, understandably, made in journals or at conferences that focus on the reliability aspects of the work. Sadly, this often means that the descriptions of the details of the surface finish processes may be incomplete and that readers of a study may assume that a conclusion is general to all surface finishes of a particular class, when it may only be true for the particular variant examined.

Given that solder joint reliability issues are often very specific to details of the surface finishes, authors of such publications could put their information in a more valuable context if they were to include more complete descriptions of the processes and material properties.

Test panel or final product reliability studies are expensive, complex and not usually appropriate for routine quality control.

Suppliers of surface finishes, whether for PWBs or for leaded or SMT components, usually use processability or solder reflow level testing for internal product development, characterization and quality control.

Data published by surface finish suppliers is generally provided with complete details of the specific products and process used. For example, information on electroless nickel deposit compositions or thicknesses of OSP coatings might be provided.

The relative ease of use of these tests is offset by the difficulty in determining whether the test results are relevant to a specific failure mode.

Planning for the Future

Material suppliers are always willing to cooperate with PWB fabricators and their customers to develop test panel or product level information on their surface finish products. Data from such studies represent the best combination of well characterized surface processes and test structures that are representative of real world products.

The best way to make sure that tomorrows cell phones and PDAs will survive their inevitable tumbles is for materials suppliers to build stronger, cooperative relationships with PWB fabricators, OEMs and OEMS, with the aim of enhancing industry understanding of the relationship between surface finishes and solder joint reliability.

References

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Further Reading

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Martin Bayes is a Research Fellow in the Circuit Board Technology group of Rohm and Haas Electronic Materials (Marlborough, MA). He may be reached at mbayes@rohmmaas.com

Rohm and Haas Electronic Materials supplies a broad range of final finishes, including electroless nickel immersion gold (ENIG), electroless nickel electroless palladium immersion gold (ENEPIG), electrolytic nickel-gold and immersion tin products.