

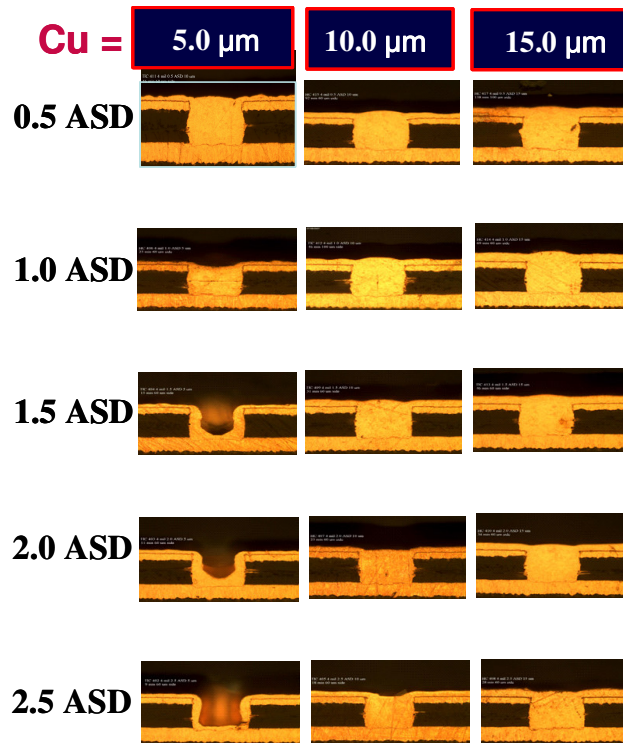
**ROHM AND HAAS ELECTRONIC MATERIALS
INTERCONNECT AND FINISHING TECHNOLOGIES**

Technical Communications

Optimum Design of Blind Via Technology

February 2009

This Article is currently published at PCB 007 website



Optimum Design of Blind Via Technology

Mass production of High-Density Interconnection (HDI) printed circuit board still faces some issues. These include problems with end-product reliability and defective external appearance, resulting in increased rework or inspection costs and customer complaints.

Both the board designer and process development engineer must understand the technical capabilities and costs of HDI manufacturing processes and consider the impact of their design choices on production yield, while, at the same time, maintaining a balance between process cost / profit and product quality.

This article examines the product design and manufacturing process implementation cycle for high-density interconnection (HDI) printed circuit boards, starting from circuit design, then production process design, the selection of raw materials and process

equipment and continuing through final assembly.

Technology needs and challenges will be identified, based on both the capability of existing HDI processes and future trends in technology development, and approaches to meet these needs will be provided.

There are many design options available for multilayer high-density interconnection (HDI) printed circuit boards, including blind and buried vias and also build-up layer constructions and layout. Designers must also consider both internal and external layer layouts.

Options for via constructions include simple blind vias (Blind Via: Figure 1a), blind via interconnects formed within external connection pads (Via in Pad: Figure 1b) and stacked vias, often formed over filled through holes in cores (Stacked Vias: Figure 1c).

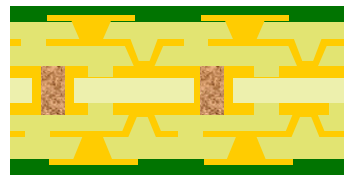
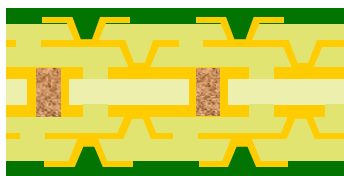


Figure 1a): Conductive Blind Via Designs

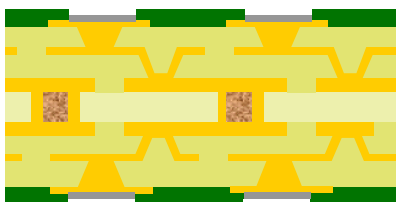


Figure 1b): Via in Pad Designs

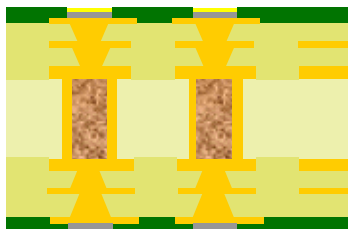


Figure 1c): Laser Stacked Vias over Filled Core Vias

In order to meet the wiring requirements of high density interconnection substrates (HDI), laser vias are required, rather than the mechanically drilled through vias used for conventional multilayer boards. Laser vias provide both smaller via diameters and

the ability to have multiple interconnects at a single X-Y location.

Table 1 shows a comparison of the capabilities of mechanical and laser drilling for via formation in multilayer PWB HDI and in integrated circuit packaging substrates.

	MLB HDI	IC Substrates
Laser Via Diameter (microns)	75 - 175	60 - 70
Mechanically Drilled Through Via Diameter (microns)	250 - 300	100

Table 1: Design rules for mechanical and laser drilling

Innerlayer Conductive Via Design

When laminating dielectric materials during manufacture of high density interconnect substrates, it is critical to ensure that all blind vias are completely filled. Should any voids be formed, they may lead to local separation between layers, or even to complete delamination, leading to product failure.

When dielectric layer thicknesses are above 70µm and via diameters are less than 70µm (i.e. via aspect ratio is above 1:1), lamination voids are more easily formed. Therefore, where possible, designers should avoid using blind via aspect ratios greater than 1:1. The production process design must consider both the depth (thickness of the dielectric material) and diameter of blind vias. The blind via plating process capability can

also have a large impact on the ability to fill vias with dielectric.

However, for products where size, weight, thickness or impedance control are critical, the designer may still have to consider the use of laser via aspect ratios above 1:1. When the laser via placement restricts routing escape density, the only design option is to reduce laser via size and via pad diameter. When trace impedance must be increased to meet design targets, a thicker dielectric layer may have to be used, thus increasing the depth of the laser vias.

During production of high aspect ratio microvia product, two approaches can be used to address the microvia reliability issues mentioned above.

The first approach is to use plating bath systems with improved throwing power capability. While normal plated via fill throwing power can only achieve around 100%, the best conformal systems can

achieve via fill throwing powers up to 130%. The rounded final via shape (shown in Figure 2) produced by these systems is more easily filled with dielectric material.

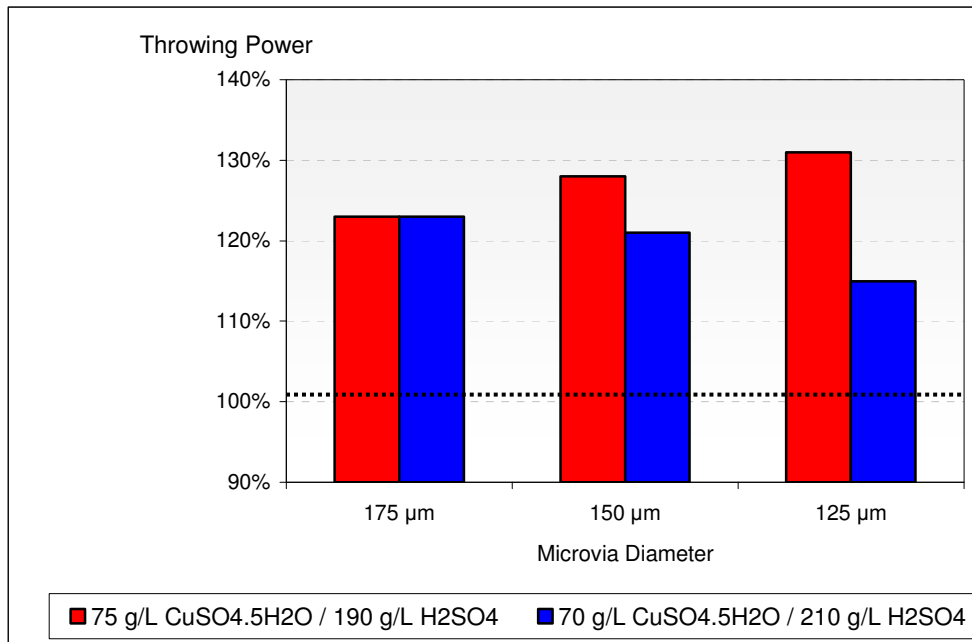
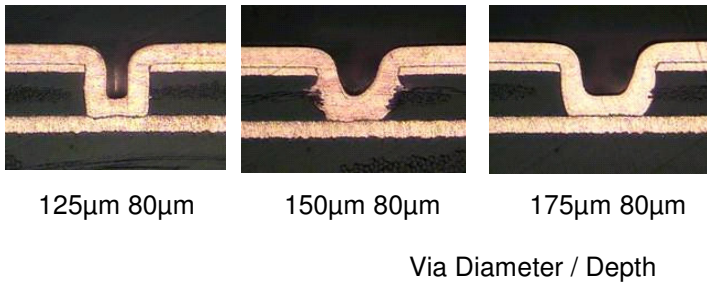


Figure 2: High Microvia Conformal Throwing Power provided by Copper Gleam™ MV-100 DC Copper Plating for HDI Applications

The second approach is to use copper filled vias to completely avoid any possibility of voids. While early generations of via filling products only had the capability to plate

products with dielectric thicknesses of 70µm, current generation production processes have been upgraded to provide plating capability for 100µm thick dielectric layers.

Outerlayer Conductive Via Design

PWB outer layer traces must be covered with solder mask, in order to avoid oxidation of the copper surface and to protect the circuit features during subsequent high temperature assembly processes. Quality issues may be encountered when applying solder mask to microvia product. The

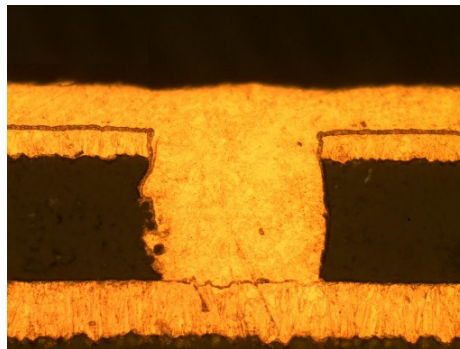
problems shown in Figures 3a (poor solder mask coverage around the microvia outside perimeter) and 3b (poor solder mask via filling) are more often seen when using dielectric thicknesses above 40µm. These two defects are considered potential product reliability issues.



Figure 3: a) Poor solder mask coverage around blind via perimeter
b) Solder mask voiding in blind via

There are a number of ways to eliminate quality problems with solder mask application to blind via product:

1. Use of traditional screenprinting methods: First, the vias should be filled with a 30µm thick layer of solder mask, before applying a second, complete layer of surface solder mask. This approach requires multiple printing operations, in order to achieve the required quality of solder mask via filling.
2. Use of a roller coater, using several passes to achieve the required level of solder mask coverage and via filling.
3. Use of a liquid solder mask vacuum printer, applying a vacuum first and then solder mask. This approach requires a long cycle time and therefore gives lower production throughput than conventional printing processes.
4. Use of a dry film solder mask vacuum laminator, first coating the substrate with dry film solder mask and then, after heating, applying vacuum to draw the mask onto the surface and into the vias.
5. Use of a plated copper via filling process to fill the blind vias. This approach both reduces the solder mask process complexity and also eliminates solder mask voids and exposed copper (Figure 4).



Via Dimensions : Diameter 100µm / Depth 100µm

Figure 4: Use of MicroFill™ EVF Copper Via Fill, a copper electroplating process, to directly fill blind vias in packaging substrates or HDI products

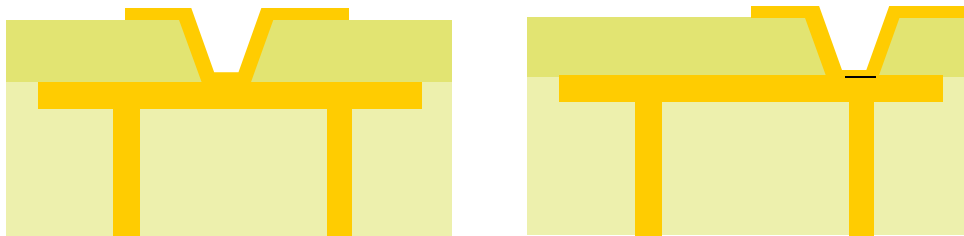
Via in Pad and Stacked Via Designs

Via in Pad and Stacked Via structures provide a greater degree of freedom in layout and allow more options for escape routing, due to the reduced number of connection points, as well as increasing the board surface area available for I/O placement.

There are a number of different types of stacked Laser Via structures. Two important examples are Laser Via on a capped through via pad (Laser Via on PTH) and Laser Via on Laser Via pad (often referred to as “free stack-up”).

However, these types of stacked via designs can be more prone to reliability issues and are more complex and expensive to fabricate. Unless very high density routing is required, designers usually choose to increase layer count, rather than use Laser Via on Pad construction.

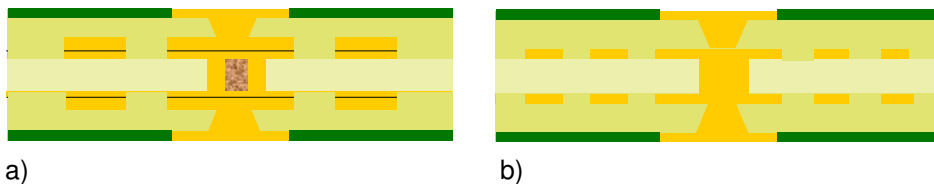
Stacked Laser Via structures require very tight control over the position of the center of the target pad, so that proper alignment of the micro via position can be achieved (Figure 5).



a) b)
Figure 5: a) Properly aligned and b) misaligned Laser Via / PTH cap pad (with interfacial failure crack caused by offset of PTH pad location)

Laser Via on PTH Pad faces particular challenges during fine line etching. The process requires two separate copper electroplating steps, one to provide copper in the vias and a second to cap the PTH vias. Even though the surface thickness can be reduced after each step, the overall thickness may still exceed 25µm (Figure 6a),

which is not conducive to fine line etching, only allowing formation of 75µm:75µm line / space features. In addition, use of a hole plugging process, followed by an abrasive grinding process, can cause dimensional changes, or layer to layer separation and may lead to increased reliability problems.



a) b)
Figure 6: a) Laser Via over Core PTH, using a two stage plating process, resulting in innerlayer copper thickness greater than 25µm
b) Combination of Filled Through Via and Blind Microvias, allowing finer line formation on innerlayers

At present, the development of filled through-hole plating, combined with a laser via on pad process, has the potential to reduce production cost and process complexity (Figure 6b), improve fine line etching capability and allow increased copper thickness in internal vias, to improve electrical and thermal performance and reduce EMI.

Laser Via on Pad is particularly suitable for double sided structures, replacing mechanical drilling, in order to improve wiring density. This approach can allow a mechanically drilled 100µm via to be replaced with a 70µm laser via, with the surface pad also providing a direct interconnection point (as shown in the 2 layer structure in Figure 1b).

Laser Via Process Control

Key variables that must be monitored and controlled in the laser via drilling process are the dielectric layer thickness, materials,

If conformal via fill plating is used, the external microvias will still face the potential problems, shown in Figure 3, of solder mask voids and poor solder mask coverage around microvia edges. The best solution is to use copper via filling to completely avoid solder mask issues, and at the same time, allow pads to be placed on both the top and bottom of the panel, thus providing more flexibility in component placement.

While stacked via structures increase design freedom, the greatest challenge remains reliability. Stringent process control is required to eliminate the risk of reliability problems. This is such a serious issue that, if not properly controlled, manufacturers may be required to shut down a production line.

process capability / stability (C_p/C_{pk}) and hole shape (Figure 7).

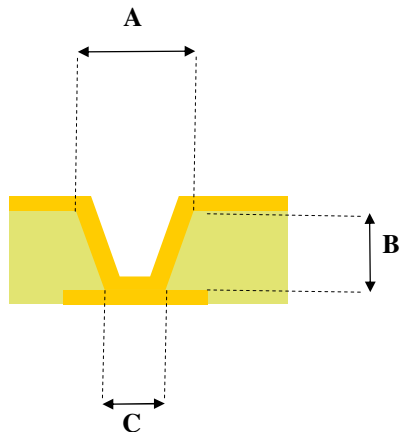


Figure 7: Key factors influencing laser via formation

1. Strict control of the laser via bottom diameter (A) to ensure sufficient adhesion between the bottom surface of the via and the pad, and also ensure that the base of the via is completely clean.
2. Control of the diameter of the top of the via (C) to be slightly larger than the base diameter, to ensure a hole shape which can be reliably plated.
3. Minimal variations in the thickness of dielectric material (B), to ensure that the laser via drilling process can deliver consistent via dimensions and reliable contact to the target pad.
4. Ensuring proper registration, when forming stacked laser vias.

Overall process monitoring, including AOI inspection, tensile testing (Figure 8), daisy chain board testing, reliability testing and electrical interconnection / impedance

testing is required to ensure that the product quality consistently meets requirements.

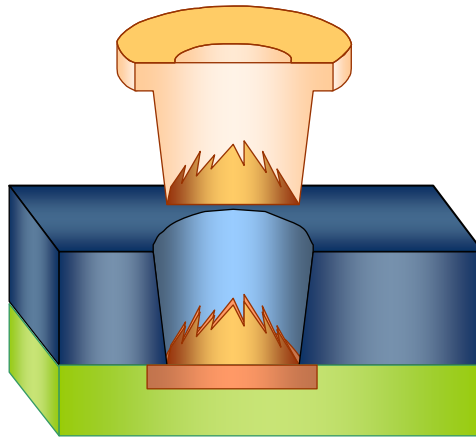


Figure 8: Blind via adhesion pull test – desired failure mode within electrolytic copper

Applications for Via in Pad

Via in Pad designs are used for wire bonding and BGA ball pad substrates, SMT passive component mounting and for thermal dissipation applications. Depending on the specific application, a number of different surface finishes may be used. Normally, wire bonding applications require

a nickel-gold surface finish, while FCBGA uses an immersion tin or ENIG surface finish. Surface mount component pads usually use either OSP or nickel-gold, while thermal dissipation pads are generally designed to have nickel-gold surfaces. Figure 9 shows examples of designs of this type.



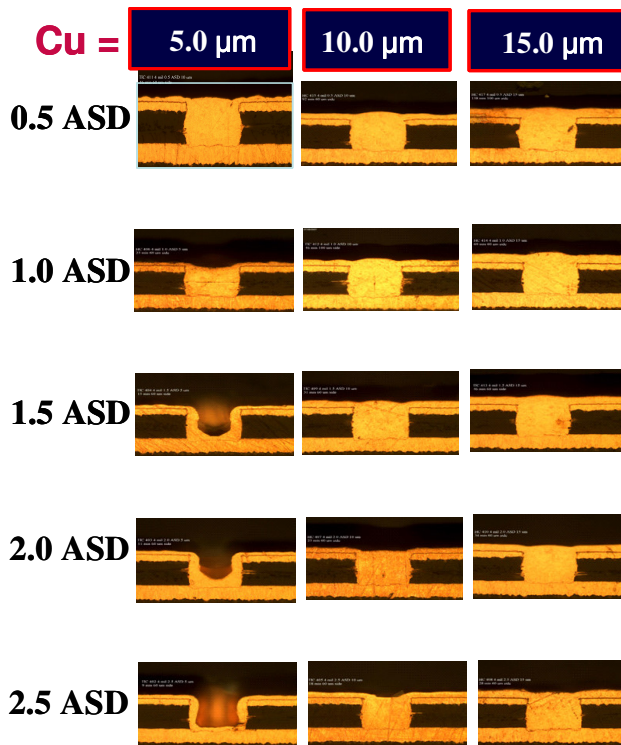
Figure 9: Via in Pad designs for BGA substrate or wire bonding applications

Possible root causes of assembly defects can include improperly applied surface finishes, or lack of process control during via fill leading to either abnormally low or high

degrees of via fill (overplate or dimpling). This can lead to solder joint voiding and subsequent cracking, or poor wire bond formation

Via in Pad applications therefore require a very smooth surface after plating, with current requirements of less than a 10µm dimple. To ensure interconnection reliability, future demands are for dimples less than

5µm, achieved with minimal surface plating thickness. These requirements can be met with products such as MicroFill™ EVF Enhanced Copper Via Fill (Figure 10).



Via Dimensions : Diameter 100µm / Depth 60µm

Figure 10: Blind via filling as a function of current density and surface copper thickness: MicroFill™ EVF Copper Via Fill

Conclusions

Use of via filling plating processes increases layout freedom and production capacity, while reducing cycle time and cost. Such processes also provide the capability to

meet future requirements for ultra-fine line and thin board technology, to satisfy end-user demands for lighter, smaller and higher performance electronic products.

References

1. M. Lefebvre, "Pattern Plate Copper Via Fill Processes for Packaging and HDI with Through-Hole Plating", CircuiTree Webinar, Original Event Date: December 9, 2008 <https://event.on24.com/eventRegistration/EventLobbyServlet?target=registration.jsp&eventid=122299&sessionid=1&key=1172D86A84F5899A1FF58423F909DB32&partnerref=website&sourcepage=register>
2. M. Lefebvre, E. Najjar, L. Gomez, L. Barstad, "Next Generation Electroplating Process for HDI Microvia Filling and Through Hole Plating", IMPACT/EMAP 2008.

Julian Chu is Asia Marketing Director in the Interconnect and Finishing Technologies of Rohm and Haas Electronic Materials Taiwan Ltd. He may be reached at julianchu@rohmmaas.com.

Rohm and Haas Electronic Materials LLC is a global supplier of a comprehensive range of printed circuit fabrication products, including dielectric pretreatment and metallization and a full range of via filling processes for HDI and packaging substrate applications.