DOW ELECTRONIC MATERIALS

INTERCONNECT TECHNOLOGIES

MEETING THE CHALLENGE OF NEXT GENERATION HDI AND PACKAGING SUBSTRATE MANUFACTURING PROCESS

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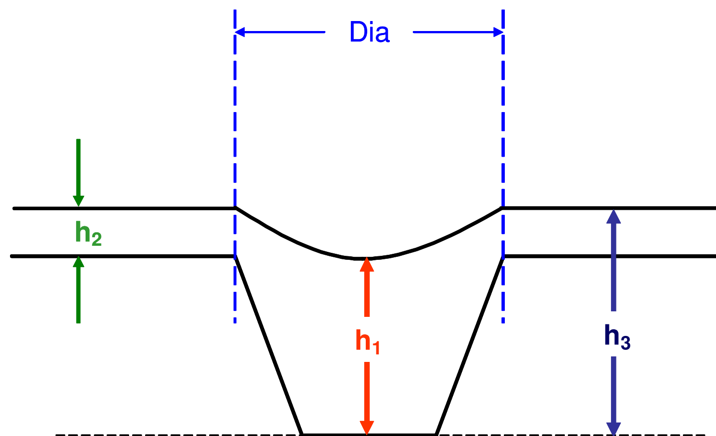

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Abstract

The use of electrodeposited copper for filling blind microvias has grown rapidly to become a key enabling technology within both Printed Circuit Board (PCB) and package substrate manufacturers. Driven by the need for increased system speed, portability and wiring density, the interconnect pitch on both semiconductor packages and High Density Interconnect (HDI) substrates continue to shrink. To keep up with these evolving needs, thinner and more uniform surface copper deposits have to be produced and increasingly difficult microvia geometries must be filled, while maintaining plating rates capable of delivering commercially acceptable production throughputs. These demands often place severe stresses on the capability of current commercial copper electroplating systems.

The features, development, scale-up of and results from a new pattern plate direct current copper via fill process are discussed.

Introduction

Driven by the need for increased speed, portability and wiring density, the interconnect pitch on semiconductor packages and the corresponding High Density Interconnect (HDI) substrates continue to shrink. The combination of filled blind microvias and build-up technology provides a means to achieve the required wiring densities. With the rapid growth of this technology, the use of electrodeposited copper for filling blind microvias has become a widely adopted process for manufacture of both HDI printed circuit boards and also semiconductor package substrates.

In order to produce the increasingly narrow line widths and spacing (L/S), required to route state of the art packages, build-up technology is undergoing a shift from subtractive techniques towards Semi-Additive Process (SAP). This shift is being driven by the inherent limitations of subtractive processes etch resolution.

In Semi-Additive processing of build-up dielectrics, a photoresist pattern is formed after initial electroless metallization of the dielectric material. Following electroplating and resist stripping, the use of a “differential etching” process allows feature formation without the use of a metal etch resist.

A modified SAP process, also referred to as Advanced-Pattern Process, is often used in HDI fabrication. In this case, a laminate coated with a thin copper foil is used for the starting material, rather than a bare dielectric.

Both of these processes are preferred over subtractive approaches due to their improved etch capability at feature dimensions below 40 microns.

Table 1. Process Technology L/S Comparison

	Subtractive Process	Pattern Process	Advanced-Pattern Process	Semi-Additive Process
Dielectric Materials	BT / FR-4 / FR-5	BT / FR-4 / FR-5	BT / FR-4 / FR-5	ABF
Cu foil thickness	12 µm	12 µm	3 µm	0 µm
L/S @ 15 µm Cu	~ 40/40 µm	~ 35/35 µm	~ 20/20 µm	~ 15/15 µm
L/S @ 25 µm Cu	~ 75/75 µm	~ 50/50 µm	~ 35/35 µm	-

With feature dimensions become smaller (both microvia diameter and trace width), and the increased reliance on pattern plating processes, the ability of copper electroplating processes to consistently produce void-free copper filled microvias, while still producing traces with acceptable cross sectional profiles, comes under increasing pressure.

This article introduces a novel copper electroplating process, capable of meeting the most demanding targets for copper via fill and trace profile. The relationships between key variables and performance will be described.

Copper Electroplating

The vast majority of via fill electroplating baths are based on electrolytes consisting of copper sulfate and sulfuric acid. Combining low cost and convenient operation, these sulfate based systems are a well established technology, having now been used in the PCB industry for over 50 years and for via fill applications for over 10 years

Inorganic Components

A typical acid sulfate system contains copper sulfate (the primary source of cupric ions), sulfuric acid (for solution conductivity) and chloride ion (as a co-suppressor). Of these components, copper sulfate, typically at concentrations above 200 g/L, has the most significant affect on via filling ability.

Organic Components

Acid copper sulfate system operated without additives typically yield deposits of poor physical properties. Organic additives, typically consisting of materials described as brighteners, suppressors and levelers, are therefore used to further refine deposit characteristics.

Suppressors, also referred to as carriers or inhibitors, are typically large molecular weight polymers that work in conjunction with small amounts of chloride to form a surface film on the plating surface, which retards the plating reaction. This limits the lifetime of individual growing grains, causing the deposit grain size to become smaller than that obtained without carrier. Carriers are present in relatively high concentration (≥ 500 mg/L) and show relatively low sensitivity to variations in the rate of mass transfer to the surface. However, in the absence of additional additives, deposits from such formulations do not have smooth, bright surfaces.

Brighteners are typically small molecular weight sulfur-containing compounds that locally increase the plating reaction by displacing adsorbed carrier. The impacts of brightener additions occur preferentially at points of lower field density, typically in surface recesses or at the bottoms of vias or trenches. The function of the brightener is to locally accelerate the rate of the copper plating reaction and further refine the grain size of the deposit.

Levelers, a further class of additives, act as selective suppressors and typically operate at low concentration (< 10 mg/L). At these low concentrations, the activity of levelers is much more mass transfer dependent then that of carriers, with the consequence that less isolated locations (such as the panel surface) are more suppressed than more isolated locations (such as the interior surfaces of vias and recesses within via hole walls).

Bottom-Up Fill Mechanism

In order for blind vias to be filled with a high quality continuous copper deposit, the plating rate within an individual via must vary. The plating rate at the base of the via must be substantially faster than that that of the remaining areas, in order to avoid premature closure of the mouth of the via opening and the consequent formation of voids or seams.

Bottom-up via filling behavior is attributed to the action of organic additives. The neutral charge suppressor rapidly forms a current inhibiting film on the Cu surface. This film has little geometric dependence due to high suppressor solution concentration. The accelerated bottom-up fill behavior is due to a local relative accumulation of brightener species at the base of the feature. As surface area in the via is reduced during deposition, the concentration of brightener species increases (1). This local concentration of brightener accelerates the plating rate relative to the surface. The leveler acts to suppress the plating at the corners of vias, and aid in reducing the formation of a void.

Via Fill and surface planarity metrics

Via filling performance may be characterized by a number of related metrics. Percent via fill (% VF) and "dimple depth" have been perhaps the most commonly used metrics used to quantify via filling performance. The relative deposition thickness (RDT) is a more recently developed metric (2). Defined as the ratio of the fill thickness and the copper thickness plated on the board surface, it is an improved indicator of filling performance. A conformal plating process will give an RDT value of 1, based on the definition shown in Fig. 1. However, even a plating formula with a filling capability of 100% may exhibit a low RDT value, perhaps as low as 2 or 3, meaning that, while the plating formula is able to fill the microvia in a bottom-up mode, the required surface thickness buildup of copper will be excessive. Higher surface thicknesses of copper detract from the ability to subsequently etch fine circuit traces.

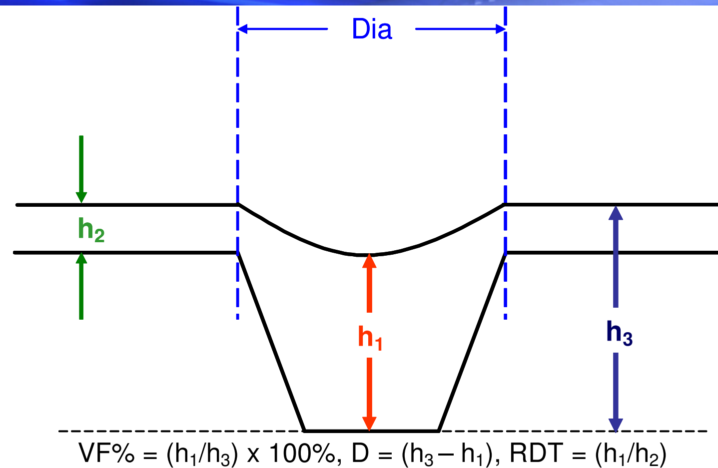

Figure 1. Definition of percent via fill (VF%), dimple depth (D) and relative deposition thickness (RDT)

In addition, for pattern plate processes, individual pad and trace features will not be perfectly flat. Trace profile is used as the general term to describe such deviations from planarity. Depending on the chemistry and process conditions, either convex or concave profiles may be formed. Customer specifications for trace profile are typically expressed as the maximum difference in height between the edge and center of a feature.

Customers are demanding continuously improved surface planarity, whether expressed as reduced dimple depth, improved trace profile or better surface distribution.

Poor planarity can potentially impact reliability in a number of ways. Dimpling can increase the effective aspect ratio of the next via formed within a stack, may lead to interfacial voiding during subsequent application of build-up dielectric, and increased risk of solder joint voiding on via in pad structures. Poor feature profile or surface distribution may lead to unacceptable variability in trace impedance, adversely affect solder mask application and may also affect wire bond consistency.

Copper Via Fill Development

The program for copper via fill process development was initiated in the Dow Electronic Materials research labs in Marlborough, MA. Product development objectives focused on maximizing via fill and through hole throwing power while minimizing thickness variation across the substrate surface. Commercially desirable via filling processes will therefore demonstrate a combination of high filling performance, low dimple and feature profile, with uniform surface distribution and high through hole throwing power. The exact target values for these metrics will depend upon specific application and end-user requirements, however for purposes of benchmarking development progress, the following performance targets were used:

- HDI: 75 – 125 µm dia x 50 – 100 µm deep
  - < 10 µm dimple @ 20 µm surface Cu
- Package Substrate: 50 – 75 µm dia x 30 – 40 µm deep
  - < 5.0 µm dimple @ 15.0 µm surface Cu
- Operating current density: 10 – 20 ASF for panel and pattern plate
- Compatible with insoluble anodes
- Through hole: 0.15 – 0.3 mm dia x 0.8 – 1.0 mm
  - ≥ 80% throwing power
- High knee thickness
- Trace and pad profile exhibit a convex track of less than 5 µm
- Panel surface distribution Coefficient of Variance (CV x 100%) ≤ 10%
- Cyclic Voltammetric Stripping (CVS) analysis for all components

Next generation HDI via filling systems should be capable of plating as wide as possible range of products with a single process chemistry, irrespective of microvia dimension or aspect ratio. Performance for different classes of product can be optimized by using specific recipes of current density and/or solution flow, and the impacts of these parameters are described later.

During the development program extensive screening was conducted of various classes and combinations of additives, carriers and levelers for via filling, trace profile an through hole throwing power performance. Candidate materials were further optimized with inorganic chemistry component concentration. Test vehicles included panel and patterned substrates featuring CO_2 and UV laser ablated blind micro vias ranging from 75 µm to 150 µm diameter and mechanically drilled through holes ranging from 0.15 mm to 0.30 mm dia in 60 µm & 100 µm thick panels.

Impact of substrate condition and pretreatment

In addition to process chemistry formulation and bath composition, complete, void free filling of blind microvias is also affected by substrate material and via profile, thickness, uniformity and oxidation of conductive seed layer and the pretreatment process.

A ‘V’-shaped via, with uniform sidewalls free of overhang or protruding glass fibers, promotes consistent seed layer formation and enhances subsequent electrolytic copper via fill. A range of via profiles is given in the schematic below, arranged to show increasing filling difficulty from left to right.

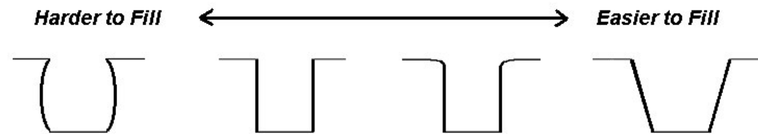

Figure 2. Microvia profile effect on ease of filling

The thickness, coverage and surface condition of the electroless copper has a profound impact on copper via filling capability. Discontinuous or overly thin electroless copper deposits will not fill as reliably as thicker, more uniform deposits. In general, uniform electroless copper deposits > 0.3 µm are required for reliable filling.

Oxidation of electroless copper can also adversely affect via fill. Previous studies showed that substrates processed with electroless copper and subsequently baked at 120ºC for several hours, failed to exhibit bottom-up fill behavior when subsequently electroplated, while panels from the same lot that were plated at the same conditions, but were not baked, exhibited normal bottom-up copper fill.(4)

Adding a conformal electrodeposited copper flash of 3 - 5 µm after electroless copper has also been shown to significantly improve process consistency, as shown by an increased tolerance to variation in hold time prior to copper via fill, as well as an improvement in overall via fill uniformity.

Proper control of pretreatment processes also plays an important role in achieving good via filling yield. A typical process sequence uses acid cleaner, micro-etching and acid dip steps to ensure that copper surfaces are completely wetted and free of contamination or surface oxidation prior to the subsequent copper plating step.

Impact of Mass Transport and Current Density

In addition to process chemistry and substrate condition, mass transport and current density has a significant impact on via filling capability. As previously mentioned, correct selection of these parameters will widen the range of microvia dimension and aspect ratio that can be produced by a single process chemistry. To understand how to best exploit these parameters, extensive testing to characterize the effects of solution agitation and current density on viafilling was conducted.

In general, lower levels of solution flow were found to improve via filling performance, particularly in large diameter vias (100 µm or above). However, this improvement comes at the price of increased risk of improperly filled smaller diameter vias (75 µm or less). Improper fill may lead to defects ranging from “seams” within the plated deposit, to completely voided vias. The consequence of this behavior is that solution flow must be carefully chosen to achieve the best balance between levels of fill and plating quality for the specific applications being run.

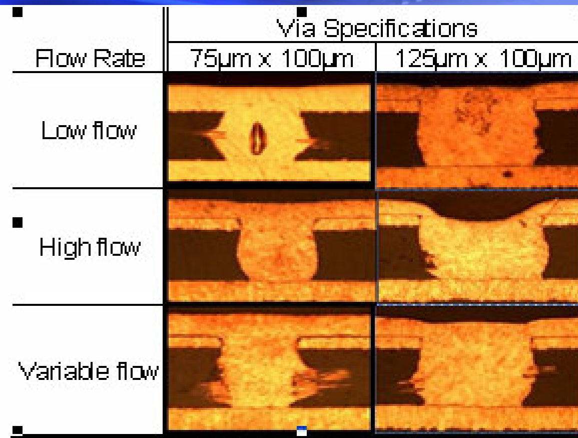

Figure 3. Via fill as a function of solution flow rate (at 18 ASF and 20 µm copper thickness)

The effects of current density are somewhat less complex. Lower current density will both enhance via filling performance and also produce product with lower levels of improperly filled vias. However, the impact of current density is strongest at the very early stages of via filling. Once vias have been partially filled, the current density may be raised without adverse effects.

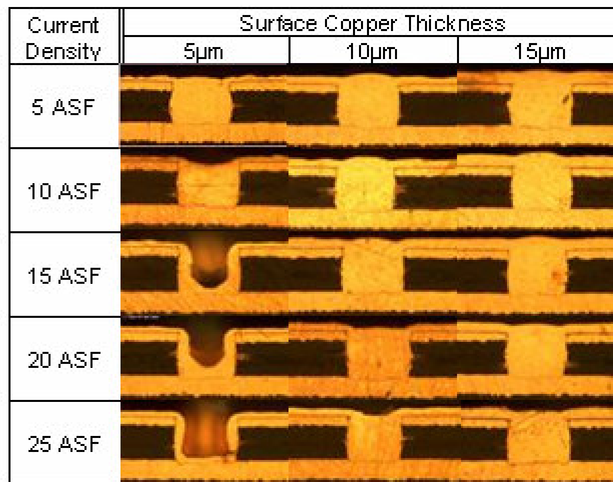

Figure 4. Via fill as a function of current density and deposition thickness (for 100µm diameter x 60µm deep via)

The use of a current density ramp from low to high, to provide the best balance between filling performance and process productivity, takes advantage of this effect.

Use of even more complex operating schemes, incorporating both variable flow and current density at different times in the plating cycle, can further improve via filling quality and raise overall production throughput.

Production Equipment

A wide variety of system design features that further enhance via filling performance may be incorporated in both batch and continuous conveyorized plating equipment. These include the use of insoluble anodes and engineered fluid delivery devices such as eductors or nozzles designed to create impinging flow on panel surfaces. Insoluble anodes improve plating uniformity by presenting a more stable anode profile over time than copper anodes. Coupled with increased solution flow, insoluble anodes also allow the use of higher operating current densities.

Considering all the different factors that influence process selection for copper via filling, careful design and selection of plating equipment with new process chemistry can provide the end user high process capability with attractive equipment cost.

Process Capability – Via Fill

For HDI applications, combining filled micro vias with conventional through holes, a proper combination of via filling and throwing power is critical.

Electrolytes optimized for micro via filling require high copper concentrations. As a result, these baths must contain lower acid concentrations, to solubilize the copper.

Electrolytes optimized for throwing power normally contain lower copper concentrations and higher concentrations of acid.

The compositions of via filling baths which must also plate through holes are slightly adjusted from the ideal compositions for via filling performance, so as to achieve sufficient through hole throwing power.

For HDI applications involving both microvias and through holes, an electrolyte containing 200 g/L copper sulfate and 100 g/L sulfuric acid is therefore preferred. For applications without through holes, an additional benefit can be obtained by using an electrolyte containing 220 g/L copper sulfate and 50 g/L sulfuric acid.

Copper sulfate	165 g/L	200 g/L	220 g/L
Sulfuric acid	145 g/L	100 g/L	50 g/L
Chloride ion	50 mg/L	50 mg/L	50 mg/L
100 µm Dia / 100 µm Thk			
125 µm Dia / 100 µm Thk			
150 µm Dia / 100 µm Thk			

Figure 5. Via fill as a function of $CuSO_4.5H_2O$, H_2SO4 concentration (at 18 ASF and 20µm copper thickness)

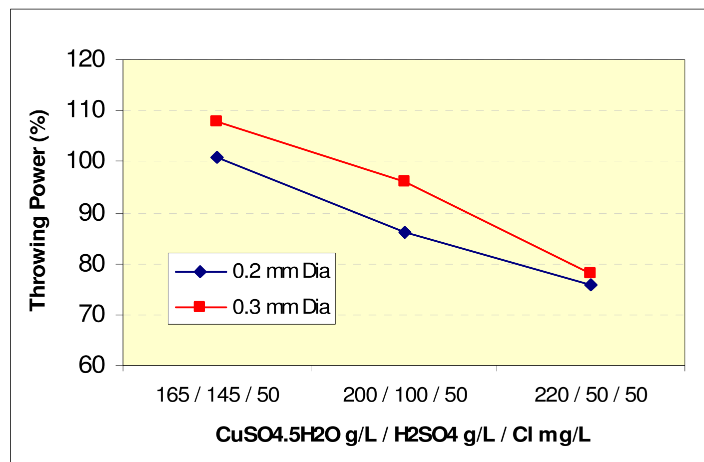

Figure 6. Through hole throwing power as a function of $CuSO_4.5H_2O$, H_2SO4 concentration (at 18 ASF and 20µm copper thickness)

Process Performance for HDI Applications (Microvias and Through Holes)

These applications require excellent micro via filling performance combined with strong through hole throwing power. These targets must be achieved while meeting surface planarity and distribution requirements. Bath performance must also be maintained as the bath is cycled.

Figure 7 demonstrates the broad via filling capability of the process that has been tuned for plating through holes. A dimple depth of less than 10 µm is achieved across a wide range of microvia dimensions with a deposition thickness of 20 µm.

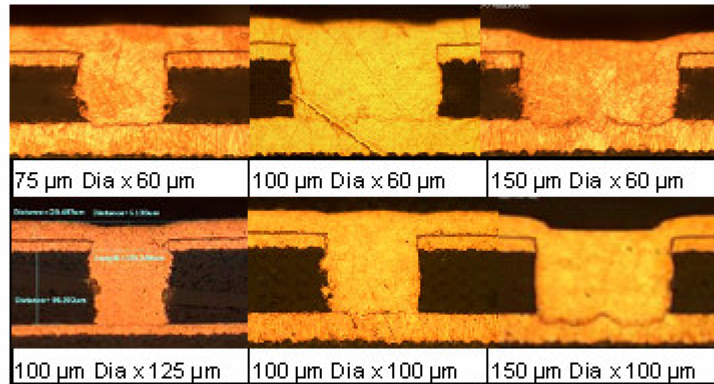

Figure 7. Fill performance over a range of microvia dimensions, (at 18 ASF and 20µm copper thickness, parameters tuned for though hole plating)

The impact of bath aging on 125 µm diameter microvias shown in Fig. 8. Test panels were processed in a production scale plating cell at bath ages from 0 to more than 300 AH/L. Consistent via fill was maintained throughout the test across a full range of microvia dimensions.

Bath life	Via specifications					
	75 µm dia / 60 µm deep	100 µm dia / 60 µm deep	125 µm dia / 60 µm deep	100 µm dia / 100 µm deep	125 µm dia / 100 µm deep	150 µm dia / 100 µm deep
200 AH/L						
250 AH/L						
300 AH/L						

Figure 8. Fill of 125 µm diameter microvias as function of bath age and dielectric thickness, (at 25 ASF and 20µm copper thickness)

HDI substrates of this type are commonly intended for applications where minimum size and weight is critical. Typical substrates are in the 1.0 mm thick range and contain hole sizes as small as 0.15 mm

Figure 9 shows the throwing power performance of the system for hole sizes from 0.2 to 0.3 mm in a 1 mm thick panel in a vertical batch jet agitation plating cell. Even at a current density of 25 ASF, excellent throwing power is achieved.

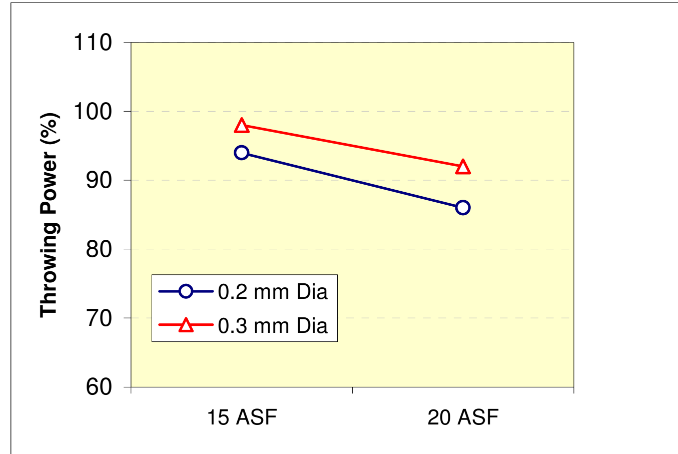

Figure 9. Through hole throwing power as a function of current density and hole diameter in production vertical in-line plating cell (for 1.0 mm thick panel at 20 µm thickness)

While first generation microvia filling processes were intended for panel plate processes, and were generally not suitable for pattern plate process applications, this process may be used in either panel or pattern plate processes.

Figure 10 demonstrates the capability of the process to simultaneously fill microvias and plate through holes when used in a pattern plate mode.

Figure 10. Through hole throwing power > 80% (for 5:1 AR through hole at 18 ASF and 20µm copper thickness)

The typical line/trace profiles that can be achieved with the novel via fill process are shown below as a function of flow and current density. These profiles show excellent planarity.

Current Density	Solution Flow	L/S (50/75 um)	L/S (50/75 um)	L/S (50/75 um)
15 ASF	Low Flow			
18 ASF	Low Flow			
DC Ramp	Low Flow			
18 ASF	High Flow			

Figure 11. Effect of flow and current density on profile (at 18 ASF and 20µm copper thickness)

Physical Properties and Interconnect Reliability

Table 2 below shows the interconnect reliability of plated through holes and blind microvias from a production next generation copper via fill process.

Figure 12 summarizes the tensile and elongation values obtained with copper via fill as a function of current density.

Table 2. Microvia and through hole intereconnect reliability

Test Item	Test Condition	Specification	Result
Thermal stress test	260ºC / 20 sec / 10 cycles	No cracks	Pass
IR reflow test	Line speed: 0.76 m/min 180ºC-180ºC-260ºC 10 cycles	No cracks	Pass
Air to air thermal shock	-40ºC / 15 min to 125ºC / 15 min 1000 cycles	Impedance variation < 10%	Pass

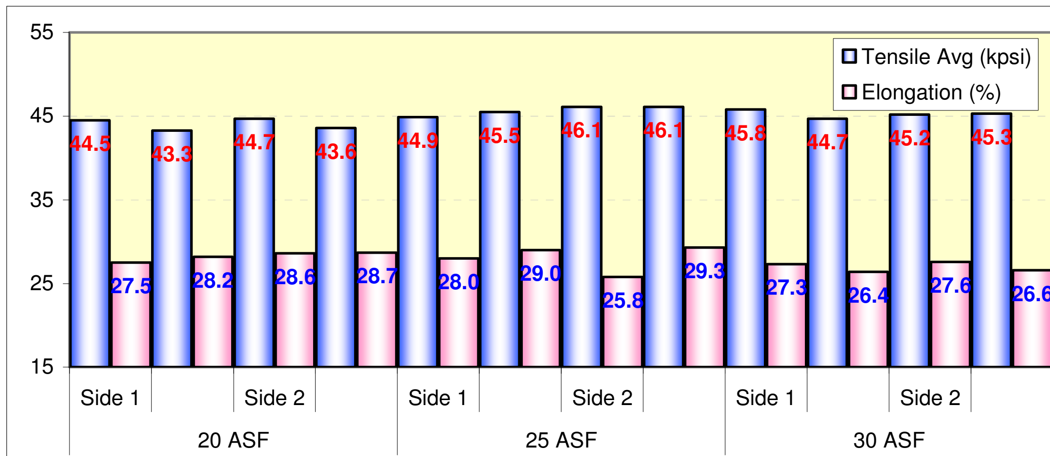

Figure 12. Deposit physical properties as a function of current density

Microvia Fill Without Through Hole Plating

For those applications that do not require through hole plating, microvia performance may be further enhanced by increasing the copper concentration from 200 to 220 g/L copper sulfate and reducing sulfuric acid concentration from 100 to 50 g/L. Even at copper deposition thicknesses as low as 10 to 12 µm and at current densities as high as 25 ASF, excellent fill performance can be achieved.

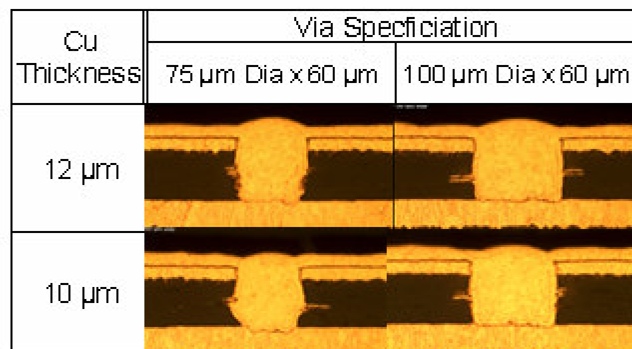

Figure 13. Via fill as a function of Cu plating thickness, (at 25 ASF)

Summary

The improved performance of a second generation via filling process provides previously unattainable levels of microvia filling and surface planarity, high through hole throwing power and pattern plate compatibility. In addition the copper via fill operating parameters can be further adjusted to maximize performance for specific end user requirements.

Combining these newly developed electroplating products with production equipment specifically engineered for via fill, provides fabricators with a system capable of meeting current needs for IC package and HDI substrate and also satisfying future roadmap targets, using proven technology for mass production of electrodeposited micro via filling.

References

1. T.P. Moffat, J.E. Bonevich, W.H. Huber, A. Stanishevsky, D.R. Kelly, G.R. Stafford, D. Jossel, “Superconformal Electrodeposition of Copper in 500 – 90nm Features”, J. Electrochem. Soc., Vol 147, 4524 (2000)

2. W.P. Dow, M.Y. Yen, M.J. Lefebvre, “Studies of Microvia Filling Mechanism and A Novel Cu Plating Formula”, IMPACT 2007

3. W.P. Dow, H.S. Huang, M.Y. Yen, H.C. Huang, “Influence of Convection-Dependent Adsoprtion of Additives on Microvia Filling by Copper Electroplating”, J. Electrochem. Soc., Vol 152, (6) (2005)

4. M. Lefebvre, G. Allardyce, M. Seita, H. Tsuchida, M. Kusaka, S. Hayashi, “Copper Electroplating Technology for Microvia Filling”, Circuit World, Vol 29 No. 2, 2003