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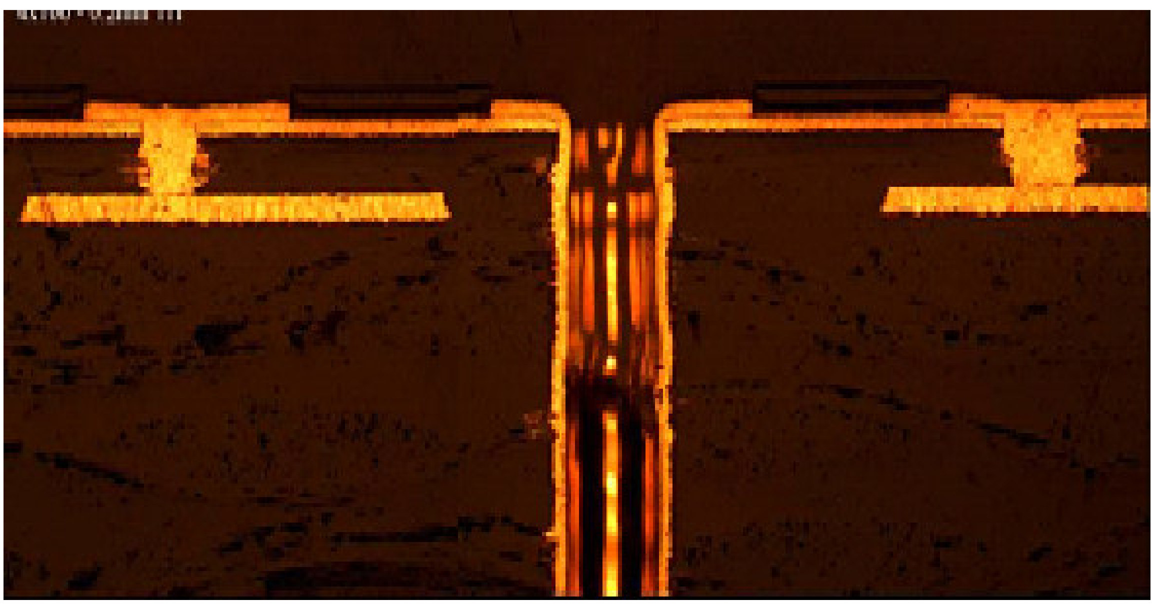

Next Generation Electroplating Technology for Microvia Filling

Introduction

Driven by the need for increased speed, portability and wiring density, the interconnect pitch on semiconductor packages and the corresponding High Density Interconnect (HDI) substrates continue to shrink. The combination of filled blind microvias and build-up technology provides a means to achieve the required wiring densities. With the rapid growth of this technology, the use of electrodeposited copper for filling blind microvias has become a widely adopted process for manufacture of both HDI printed circuit boards and also semiconductor package substrates.

In order to produce increasingly fine pitch designs, build-up technology has shifted from subtractive techniques (which are limited by etch process tolerances) towards Semi-Additive Processing (SAP). As both microvia dimensions and trace widths become smaller, the ability of copper filling processes to consistently produce void-free copper filled microvias and traces with acceptable cross sectional profiles comes under increasing pressure.

This article describes a number of key factors affecting copper electroplating for microvia filling and the levels of performance that are currently available to meet the needs of this important market.

Bath Chemistry Parameters Affecting Via Fill

The vast majority of via fill electroplating baths are based on electrolytes consisting of copper sulfate and sulfuric acid. Combining low cost and convenient operation, these sulfate based systems are a well established technology, having now been used in the PCB industry for over 50 years and for via fill applications for over 10 years.

A typical acid sulfate system contains copper sulfate (the primary source of cupric ions), sulfuric acid (for solution conductivity) and chloride ion (as a co-suppressor). Of these components, copper sulfate, typically at concentrations above 200 g/L, has the most significant affect on via filling ability.

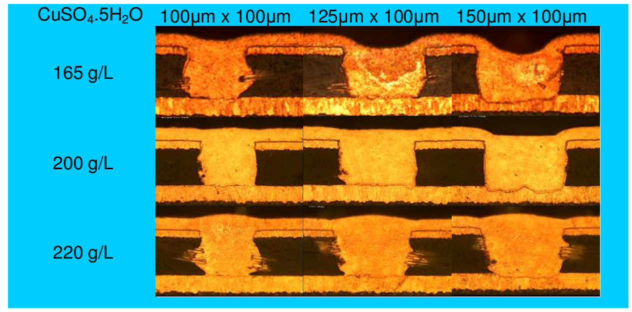

Figure 1. Via fill as a function of $CuSO_4.5H_2O$ concentration (at 1.8 ASD and 20µm copper thickness)

Acid copper sulfate system operated without additives typically yield deposits of poor physical properties. Organic additives, typically consisting of materials described as brighteners, suppressors and levelers, are therefore used to further refine deposit characteristics.

Carriers are typically large molecular weight polymers that work in conjunction with small amounts of chloride to form a surface film on the plating surface, which retards the plating reaction. This limits the lifetime of individual growing grains, causing the deposit grain size to become smaller than that obtained without carrier. Carriers are present in relatively high concentration (500 – 3000 g/L) and show relatively low sensitivity to variations in the rate of mass transfer to the surface. However, in the absence of additional additives, deposits from such formulations do not have smooth, bright surfaces.

Brighteners are typically small molecular weight sulfur-containing compounds that locally increase the plating reaction by displacing adsorbed carrier. The impacts of brightener additions occur preferentially at points of lower field density, typically in surface recesses or at the bottoms of vias or trenches. The function of the brightener is to locally accelerate the rate of the copper plating reaction and further refine the grain size of the deposit.

Levelers, a further class of additives, act as selective suppressors and typically operate at low concentration (< 10 ppm). At these low concentrations, the activity of levelers is much more mass transfer dependent then that of carriers, with the consequence that less isolated locations (such as the panel surface) are more suppressed than more isolated locations (such as the interior surfaces of vias and recesses within via hole walls).

Bottom-Up Fill Mechanism

In order for blind vias to be filled with a high quality continuous copper deposit, the plating rate within an individual via must vary. The plating rate at the base of the via must be substantially faster than that that of the remaining areas, in order to avoid premature closure of the mouth of the via opening and the consequent formation of voids or seams.

Accelerated bottom-up filling has been attributed to the mode of action of the organic additive system (1). The suppressor or carrier forms a current inhibiting film on the Cu surface. This film forms uniformly at all locations, assisted by the high solution concentration of suppressor. The accelerated bottom-up filling (i.e. “superfilling”) is believed to be driven by brightener concentration enhancement at the base of the feature (via or trench) during the plating process. Progressive reductions in surface area of via bottoms during deposition “squeeze” the brightener into ever decreasing areas. This localized concentration of brightener further accelerates the plating rate relative to the surface. The leveler acts to suppress the plating at the corners of vias, and aid in reducing the formation of a void. In order to maintain bottom-up filling behavior, brightener concentration must be controlled within specified limits.

Process Parameters Affecting Via Fill

In addition to process chemistry formulation and bath composition, the key process factors affecting via filling are substrate condition, solution flow, current density and the pretreatment process.

Via profile, thickness and uniformity of the initial conductive layer, degree of surface oxidation and type of dielectric material have a significant impact on via filling ability. A ‘V’-shaped via, with uniform sidewalls free of overhang or protruding glass fibers, promotes consistent seed layer formation and enhances subsequent via fill. Accordingly, non-reinforced dielectric materials are generally easier to fill. A thin or discontinuous seed layer will significantly degrade via fill performance.

While lower levels of solution flow will generally improve via filling performance, particularly of large (100 µm or above) vias, this improvement comes at the price of increased risk of improperly filled small (75 µm or less) diameter vias. Improper fill may manifest itself as defects ranging from seams within the plated deposit, to completely voided vias. The consequence of this behavior is that equipment parameters must be optimized to achieve acceptable levels of fill and plating quality for the specific applications being run.

The effects of current density are somewhat less confounded, as lower current density will both enhance via filling performance and also produce product with lower levels of improperly filled vias. However, the impact of current density is strongest at the very early stages of via filling. Once vias have partially filled, higher current densities can be applied without adverse effects.

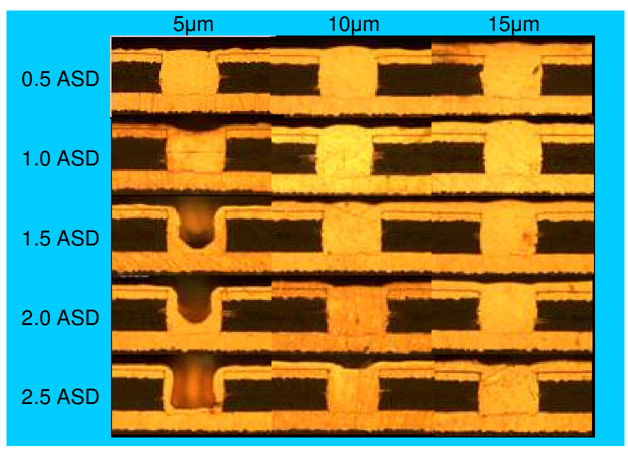

Figure 2. Via fill as a function of current density and deposition thickness (for 100µm diameter x 60µm deep via)

While the simplest way to operate a plating process might be to run a single set of flow and current density parameters, use of more complex operating schemes, incorporating variable flow and current density at different times in the plating cycle, can yield better via filling quality and higher overall production throughput.

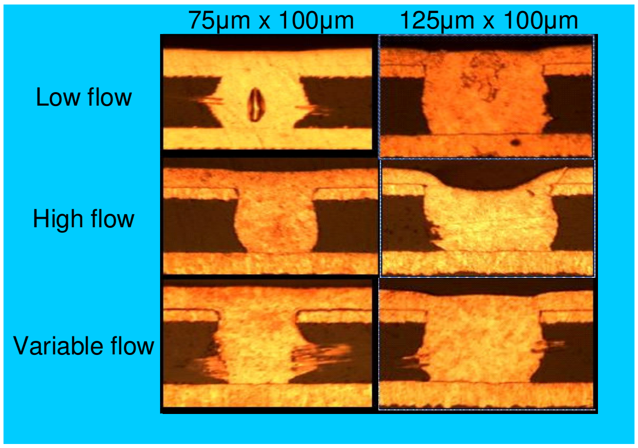

Figure 3. Via fill as a function of solution flow rate (at 1.8 ASD and 20µm copper thickness)

Proper control of pretreatment processes also plays an important role in achieving good via filling yield. A typical process sequence uses acid cleaner, micro-etching and acid dip steps to ensure that copper surfaces are completely wetted and free of contamination or surface oxidation prior to the subsequent copper plating step.

Evolution of Via Fill Metrics

Via filling performance may be characterized by a number of related metrics. Percent via fill (% VF) and "dimple depth" have been perhaps the most commonly used metrics used to quantify via filling performance. The relative deposition thickness (RDT) is a more recently developed metric (2). Defined as the ratio of the fill thickness and the copper thickness plated on the board surface, it is an improved indicator of filling performance. A conformal plating process will give an RDT value of 1, based on the definition shown in Fig. 4. However, even a plating formula with a filling capability of 100% may exhibit a low RDT value, perhaps as low as 2 or 3, meaning that, while the plating formula is able to fill the microvia in a bottom-up mode, the required surface thickness buildup of copper will be excessive. Higher surface thicknesses of copper detract from the ability to subsequently etch fine circuit traces.

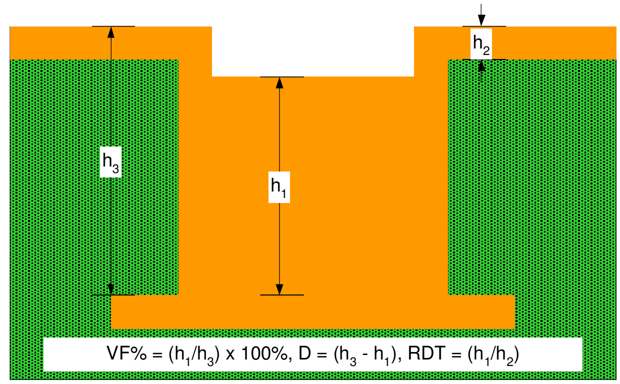

Figure 4. Definition of percent via fill (VF%), dimple depth (D) and relative deposition thickness (RDT).

Commercially desirable via filling processes will therefore demonstrate a combination of high fill %, low dimple and high RDT, with the exact values dependent upon specific application and end-user requirements.

Pattern Plating Requirements

Semi Additive Processing is the preferred method for producing build-up layers in IC package substrates. After initial electroless metallization of the dielectric material, a photoresist pattern is formed to define the final circuit pattern. Following electroplating and resist stripping, use of a "differential etching" process, allows feature formation without the use of a metal etch resist. A modified SAP process is used in HDI build-up layers, starting with thin copper foil.

These processes are preferred over conventional subtractive and pattern plating methods due to etch factor problems encountered at lines dimensions below 40 microns.

Trace and via surface profiles must be as flat as possible, to facilitate subsequent stacked via formation, overall build-up uniformity and imaging acuity. Additionally, outer layer pad profiles must be planar to allow reliable wire bonding.

50µm Line / 50µm Space | 75µm Line / 75µm Space | 100µm Line / 100µm Space

Figure 5. Effect of trace width and space on profile (at 1.8 ASD and 20µm copper thickness)

First generation microvia filling processes were intended for panel plate processes and are generally not compatible with current pattern plate process requirements. Second generation products are now available to meet these needs.

Through Hole Throwing Power

For HDI applications, combining filled micro vias with conventional through holes, throwing power is also important. Throwing power is affected both by the solution conductivity and the geometry of the through hole, primarily its length.

In contrast to via filling baths, high throwing power electrolytes are characterized by high acid and low copper concentrations, and are highly conductive. Electrolytes optimized for micro via filling are of much lower conductivity, due to the need to solubilize the required high copper concentrations. Formulations for these applications must therefore be a compromise between via filling performance and through hole throwing power.

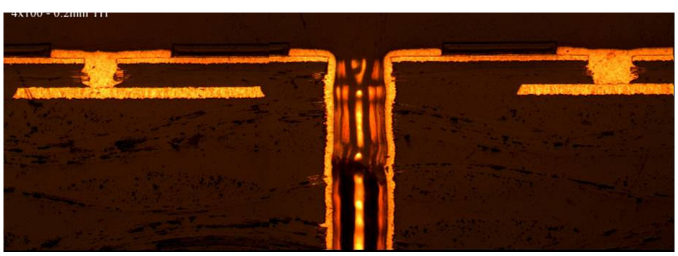

Figure 5. Through hole throwing power > 80% (for 5:1 AR through hole at 1.8 ASD and 20µm copper thickness)

Production Equipment

A wide variety of system design features that further enhance via filling performance may be incorporated in both batch and continuous conveyorized plating equipment. These include the use of insoluble anodes and engineered fluid delivery devices such as eductors or nozzles designed to create impinging flow on panel surfaces. Insoluble anodes improve plating uniformity by presenting a more stable anode profile over time than copper anodes. Coupled with increased solution flow, insoluble anodes also allow the use of higher operating current densities.

Considering all the different factors that influence process selection for copper via filling, careful design and selection of plating equipment with new process chemistry can provide the end user high process capability with attractive equipment cost.

Summary

The improved performance of second generation via filling processes provides previously unattainable levels of microvia filling, combined with pattern plate compatibility. Combining these newly developed electroplating products, with production equipment specifically engineered for via fill, allows fabricators to meet current and future needs for IC package and HDI substrate roadmap targets, using proven technology for mass production of electrodeposited micro via filling.

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