Development of a Plated Nickel Seed Layer for Front Side Metallization of Silicon Solar Cells

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Abstract

The use of a fully plated front contact for metallization of silicon solar cells, may offer significant improvement in cell performance, as compared to a screen printed and fired silver paste contact. The ability to pattern narrower grid lines, for reduced light shadowing, combined with the lower resistance of a metal silicide contact and improved conductivity of a plated deposit should combine to produce higher cell efficiencies. However, testing has shown a significant impact of upstream cell processing on the ability to consistently achieve the improvements referenced. Here we review the results of our testing and discuss options for reducing the sensitivity of the nickel seed layer process to normal variations in the upstream cell manufacturing process.

Introduction

The objectives defined at the onset of this work were as follows:

1. Develop a process for metallization of front side contact grid, using a plated nickel seed layer followed by a silver layer, deposited via light induced plating (LIP), for track conductivity
2. Investigate relationship between Ni/Ag deposit properties and sintering temperature profiles. Optimize process setting to achieve the lowest possible contact resistance, while minimizing the potential for shunting, caused by excessive Ni diffusion during sinter.
3. Optimize metallization and sintering process parameters to achieve maximum cell performance and passing adhesion of plated metal stack.

Process Sequence

The metallization sequence first investigated is shown in Table 1. Some initial testing was performed with the rear side Al paste application and firing prior to patterning of the front side SiNx, for metallization. However, the time required to etch the SiNx during patterning, was found to be significantly longer for previously fired cells, due to the densification of the SiNx layer, during firing. Therefore, the sequence shown in the table was adopted to reduce potential etch resist failure and/or increased undercut of the SiNx, during etch.

Table 1

Manufacturing Sequence with Location of Nickel Seed Layer Process Steps	
Step	Process Description
1	Wafer saw - Bulk Si + [B] ingot
2	Damage removal + Cleaning + Texturizing
3	[P] Doping diffusion
4	Oxide removal/PSG etch
5	ARC - SiNx deposition - PECVD
6	**Contact Formation**
6a	Pattern front side contact grid - inkjet/HF - etch paste - laser ablation
6b	Rear-side contact metallization - screen print Al paste
6c	Rear side contact formation - Al paste firing
6d	Metal seed layer deposition - HF activation + Ni plating
6e	LIP Ag
6f	Front side contact formation - sinter to form ohmic contact
7	Edge isolation - laser groove or wet chemical
8	Cell characterization

Metallization Process Development

When we first began our investigation of nickel seed layer processing, we had access to a limited supply of pre-patterned, monocrystalline wafers (SiNx already opened). This allowed us to perform some initial investigation of the metallization and sintering processes, prior to addressing cell patterning.

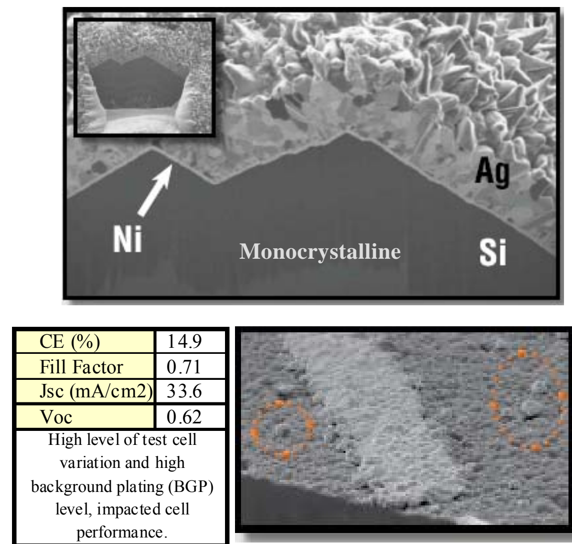
The first area of focus was to develop a nickel plating chemistry and process conditions necessary to provide a deposit of suitable thickness, and coverage uniformity, over a wide variety of cell substrates. After a thorough investigation of formulation and process effects, a suitable Ni plating chemistry and process conditions were identified. The primary criteria used to evaluate the Ni plating results, were as follows:

1. Ability to deposit a uniform, continuous plated Ni layer (as viewed by SEM imaging), within the target thickness range.
2. Adhesion of the Ni seed layer to the cell substrate.
3. Adhesion of Ag plated (LIP) layer, to the Ni seed layer.

Please note that “adhesion” here, refers to the ability to deposit the desired metal stack, with sufficient adhesion to allow continued processing up to and through sintering, without any lifting or flaking of the deposit. No process conditions were found which produced a deposit capable of passing a tape or wire pull adhesion test, immediately after plate. However, during our testing of cell substrates from several different manufacturers, it was clear that some substrates exhibited much better adhesion than others. In some cases different cell lots, from the same manufacturer, exhibited significantly different levels of adhesion, after identical metallization processing.

Optimization of the LIP Ag conditions was relatively straight forward, as we had already developed considerable experience with this process. One area that did require some additional work, was, the identification of the sequence between Ni deposition and LIP Ag, which provided the best metal adhesion.

After optimization of metallization process and conditions, a group of cells were processed to evaluate performance. Results of this testing are shown in Figure 1, below.



CE (%)	14.9
Fill Factor	0.71
Jsc (mA/cm2)	33.6
Voc	0.62
High level of test cell variation and high background plating (BGP) level, impacted cell performance.	

Figure 1: FIB/SEM Images and Performance Data

Although initial results of our testing using pre-patterned monocrystalline wafers was promising, we were concerned with the high level of “background plating” (BGP) and high level of variability in the starting wafer material. We were also anxious to explore the effects of image and etch conditions on metallization performance and to baseline performance of multicrystalline wafer material.

Patterning of Silicon Nitride for Metallization

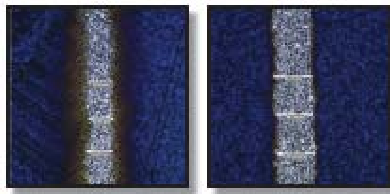
After a considerable period of optimization, including reformulation of our existing inkjet resist, we achieved a level of competence, sufficient to image and etch cells for further optimization of the metallization process. Some of the challenges faced by our inkjet formulation chemists and application engineers are outlined below:

1. Extreme variation in the density, porosity and

surface energy (contact angle) of the SiNx, antireflective coating. This extreme level of variation in the SiNx, was found, even between different cell lots, prepared by the same fabricator, using apparently identical processing conditions.

2. Significant variation in SiNx deposits produced by suppliers of different SiNx process equipment.
3. Ability of the inkjet etch resist to withstand the much longer etch times required to pattern densified (previously fired during rear side Al paste firing) vs. time required to pattern undensified (not previously fired) SiNx.
4. Optimization of image and etch conditions for patterning the smallest possible feature widths, without compromising the integrity of the etch resist, during the longer exposure times required to etch the more resistant SiNx variations

The following images provide examples of the variations described above.



LW = 55 µm LW = 85 µm

Figure 2: Similar cells with two different SiNx processes, exhibit variations in LW and undercut

After etch line width of 25 to 30 µm is within capability of inkjet process, when applied over substrate, which is compatible with optimum adhesion of the hot melt etch resist.

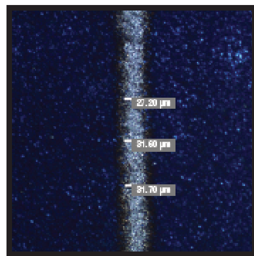
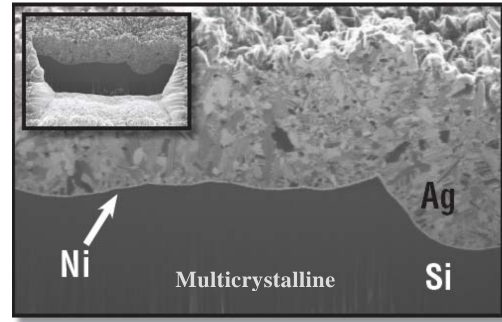


Figure 3: After LW = 30 µm with compatible SiNx

Initial Plating Results for Multicrystalline Cells

After completing the etch patterning, process work described above, a group of multicrystalline cells were plated with nickel followed by LIP Ag. Results of this testing are shown in Figure 4.



CE (%)	14.8	Jsc (mA/cm2)	30.7
Fill Factor	0.75	Voc	0.606

Figure 4: Multicrystalline Cell Performance Data

Please note the following:

1. Significant undercut when processing these samples, resulted in after plate line width (LW) of 160 µm. This was over three times greater than the target LW of 30 to 50 µm.
2. Performance values shown, were statistically indistinguishable from neighbored wafers manufactured using a full paste process, with a LW of 120 µm.

Background Plating

Cells examined prior to metallization, typically exhibit randomly located pinholes in the coating as indicated by bright spots in the nitride coating when examined under optical microscope at 500 X magnification. These bright spots indicate small openings in the SiNx coating, which when metalized, will plate in the same manner in which plating occurs in areas where the nitride has been intentionally opened. This results in metal deposition, where no plating is desired or background plating (BGP). Plating in these areas shadows light, reducing Isc values and overall cell performance. There is also a concern that the small openings in the nitride may create paths through which plated metals may diffuse through the emitter, resulting in partial or complete shunting of the cell. See Figure 5, for additional information.

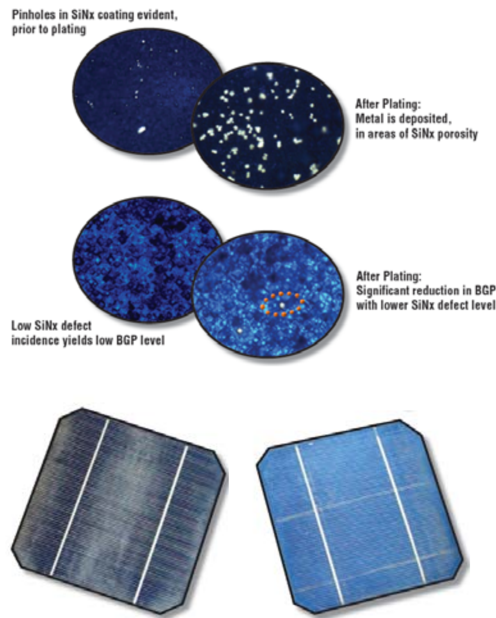


Figure 5: Background Plating caused by Defects in the SiNx

Of the challenges discussed thus far, BGP has been the most difficult to resolve, as it represents a pre-existing condition with the potential to cause severe degradation in performance of a plated cell, while having little to no impact on the same cell metallized using a screen printed paste contact. After numerous unsuccessful attempts to address the BGP problem, through formulation and process adjustments, testing of a radical change in the process sequence resulted in complete elimination of the BGP. With the elimination of BGP, came a corresponding improvement in cell performance and process latitude.

The process changes required to generate the improvements described, are outlined below:

1. Screen print and fire the rear side Al paste contact, prior to patterning the SiNx.
2. Next, apply inkjet resist and etch to create openings for front side contact grid.
3. After patterning, leave the inkjet etch resist intact, for Ni and Ag metallization. The inkjet etch resist permits sufficient light penetration to allow use of light induced plating (LIP).
4. Finally, the etch resist is removed using a stripping solution, prior to sintering.

The etch resist is highly resistant to the plating chemistries used and the pore free surface, prevents any metal deposition, in the non patterned areas. Another benefit to the use of combination etch/plating resist is that the resist constrains the ability of the plated finger to grow in width, as the plated thickness is increased. The impact of the plating resist is clearly evident in Figure 6, below:

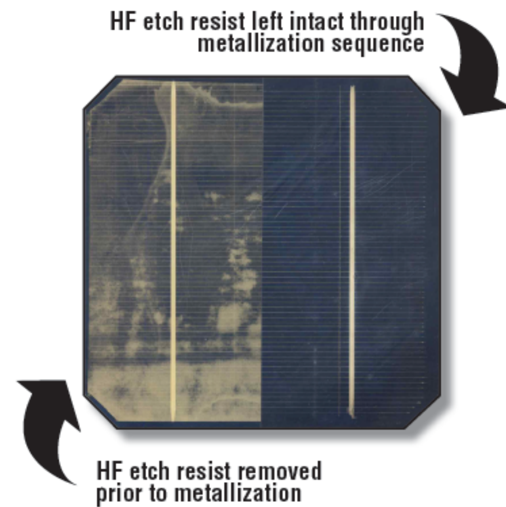


Figure 6: Effect of Plating Resist

Initial testing of the combination etch/plating resist has also produced cells of higher efficiency, Isc and post-plate shunt resistance. The plating resist not only prevents BGP over pre-existing SiNx defects, but also reduces the potential for scratches or other handling defects, to damage the nitride,

Conclusions

1. Consistent Ni coverage achieved over a variety of cell substrates.
2. Techniques developed for optimizing sintering parameters
3. Relationship between surface texture and plated metal adhesion established.
4. Have demonstrated statistically equivalent cell performance to neighbored cells processed using a standard screen printed contact grid.

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